IN THE SPECIFICATION

Please amend paragraph [0057] of the present application as follows:

[0057] FIG. 8 shows logic 800 that is one embodiment of logic 510 [[500]] of FIG. 5 for controlling a row of memory cells in array 210. Logic 800 includes NAND gates 801-803, AND gate 804, NOR gates 805-807, OR gate 808, inverters 810-814, and inputs to receive a data bit DIN, a write enable signal WR_EN, a power-on reset signal POR, a pre-charge signal PCH, a pre-discharge signal PDCH, a test signal TEST, and the write control signal WR. In response to DIN and the control signals, logic 800 generates the dataline control signals ch_dl, dch_dl, ch_dlb, and dch_dlb and the dataline driver control signals $\overline{RD}$ and WR.